Analysis and Optimization of Multisection Capacitive DACs for Mixed-Signal Processing

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***Abstract*— This paper examines the concept of multisection capacitive digital-to-analog converters (MS-CDACs), which enables a wider range of CDAC section segmentation options beyond split-CDAC and C–2C methods. In order to study the proposed approach, analysis and simulations are first conducted for all possible section arrangements of a 6-bit resolution MS-CDAC with minimum-sized unit capacitors; the study shows that MS-CDAC provides various options with reduced total capacitance compared to a single-section CDAC, and allowing for the tradeoff of area, switching energy, and speed versus static linearity and kT/C noise. Thus, it is possible to find a structure that minimizes total capacitance while satisfying required static linearity and noise that cannot be achieved with the existing methods. Compensation of nonlinearities due to parasitic capacitance is accomplished by sizing the bridge capacitance(s). To verify effectiveness in a more practical design scenario, this approach is applied to a 10-bit MS-CDAC design. Using metal–insulator–metal capacitors available in a standard CMOS technology, under the condition that 95% of Monte Carlo simulation results have at most 0.5 LSB of |DNL|, the selected 10-bit MS-CDAC structure reduces total capacitance and switching energy by 97% and 98%, respectively, and MSB capacitance by a factor of 26 relative to the single-section CDAC. The postlayout simulations were also conducted to validate the MS-CDAC approach, achieving <0.1 LSB of $|\text{DNL}|_{\text{max}}$ in the presence of additional layout parasitics.**

***Index Terms*— Analog signal processing, C–2C, charge-scaling digital-to-analog converter (DAC), split-capacitive DAC (CDAC), successive approximation register (SAR)-analog-to-digital converter (ADC).**

I. Introduction

CAPACITIVE digital-to-analog converters (CDACs), consisting of binary-weighted switched-capacitor arrays to realize voltage levels at their output corresponding to input digital codes, have been widely adopted in successive approximation register (SAR)-analog-to-digital converter (ADC) designs, as shown in Fig. 1(a) [1]–[16], and also recently used as coefficient multipliers in analog signal processing applications as depicted in Fig. 1(b) [17]. The CDAC architecture has the advantage of low power consumption, but increasing resolution demands larger capacitor arrays, which in turn negatively impacts the speed, power consumption, and area.

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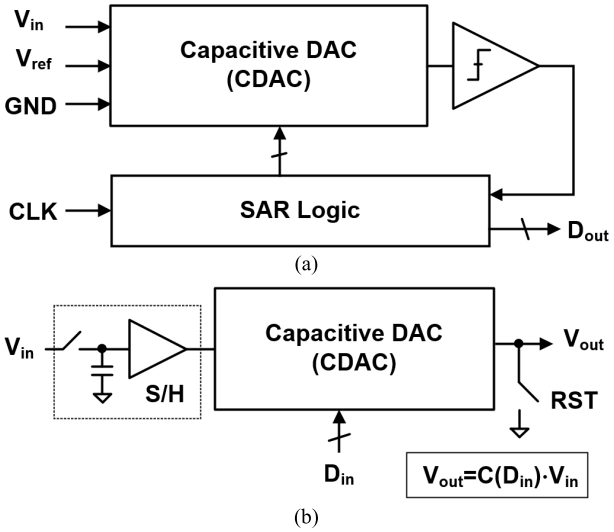


Fig. 1. Applications of CDACs. (a) SAR-ADC. (b) Analog coefficient multiplier.

The split-CDAC [1] and C–2C [2] structures were introduced to help compensate for this issue.

In the conventional CDAC design, there is a fundamental tradeoff with the size of the unit capacitor (C_U). The unit capacitor size should be minimized for the area, switching energy, and speed, but must not be too small in order to satisfy kT/C noise or mismatch requirements. Meanwhile, it is possible that the minimum capacitor available in the process limits the unit capacitor size, even if those requirements still allow the unit capacitor size to be further reduced. In this situation, the split-CDAC/C–2C structures become particularly useful as a means to further reduce the area, switching energy, and settling time with the given minimum capacitor. In practice, this is the case when SAR-ADCs of typical resolution (10–16 bit) are implemented with metal–insulator–metal (MIM) or fringe capacitors due to their excellent matching performance [3]–[5]. Although custom metal–oxide–metal capacitors can be used to chieve very small unit capacitances (few femtofarads) to overcome the minimum size limit [6], [18], their variation is not accurately estimated without testing of fabricated structures, and they also require time-consuming design efforts [5]. Moreover, the segmented CDACs reduce the number of capacitor units resulting in simplified layout and reduced overhead area, which also improves the speed performance [4].

The standard split-CDAC structure is composed of two sections with the same number of bits of switched capacitors in each section, usually called the MSB and LSB sections, while

the C–2C structure is composed of an MSB section with an array of a specific number of binary switched capacitors and an LSB section, consisting of a single-switched unit capacitor and $2C_U$ bridge capacitor pairs in series that resolves the remaining number of bits. The proposed multisection CDAC (MS-CDAC) method is an extension of the split-CDAC/C–2C concepts, with multiple sections from 2 to N, where N is the total number of bits, and with various bits in each section, yielding a range of structure options. By adopting this design approach, a CDAC can be improved with more flexible control over design tradeoffs depending on the application, which maximize the performance of the CDAC structure. There have been prior detailed analyses of conventional (two-section) split-CDACs [5], [7], [8], especially in terms of nonlinearity performance, but >2 section MS-CDACs have not been comprehensively studied. The 10-bit ADCs implemented with three section CDACs were shown in [9] but no details were provided on the CDAC design optimization. In [10], three section CDACs with varied number of bits in each section were considered but the selection was simply made for the minimum total capacitance.

The scope of this paper is to investigate the characteristics and tradeoffs of MS-CDACs and identify the optimal selection among the options for both coefficient multiplier and SAR-ADC applications. The organization of this paper is as follows. Section II introduces the general concept and underlying principles of the MS-CDAC. Section III analyzes the performance of the possible section arrangements of an example 6-bit CDAC and discusses the general characteristics and tradeoffs of MS-CDACs. Section IV provides a design example of a 10-bit MS-CDAC using the proposed approach. Finally, the conclusion is provided in Section V.

II. Concept of Multisection Capacitive DACs

CDAC is made up of an array of binary-weighted switched capacitors. The switched capacitors are usually built with unit capacitors in order to minimize the nonlinearity from mismatch. The number of unit capacitors increases exponentially with the desired number of resolution bits, which makes the interconnection of the capacitor arrays increasingly complicated and large. The MS-CDAC architecture, as with split-CDAC and C–2C methods, allows designers to avoid the large number of capacitor units by segmenting the capacitor array into the multiple sections. In order to understand the concept, we examine the two-section (split-CDAC) case before extending the analysis to more sections.

Fig. 2(a) illustrates the integration of the M-bit and L-bit binary weighted CDACs. In the M-bit CDAC structure, the leftmost capacitor is a dummy capacitor of unit capacitance (C_U) and is always connected to ground or other logic "0" reference. Due to the dummy capacitor, the LSB voltage is $V_{\text{ref}}/2^M$, and MSB voltage is exactly $0.5V_{\text{ref}}$. The L-bit CDAC section with bridge capacitor (C_B), also known as attenuation capacitor, is substituted for the dummy capacitor. C_B maintains the functionality of both sections at the same time when its value is

$$C_B = \frac{2^L}{2^L - 1} C_U. \tag{1}$$

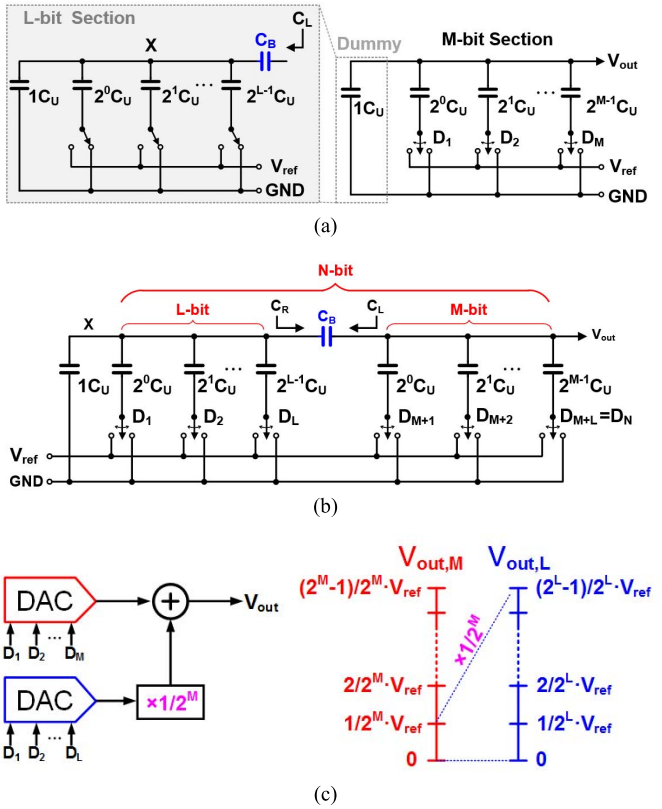


Fig. 2. Integration of two CDACs. (a) Switching a dummy capacitor with a new CDAC. (b) Two-section CDAC. (c) Equivalent description of two-section CDAC.

The resulting N-bit ($M + L = N$) two-section CDAC is presented in Fig. 2(b). Given C_B, the capacitance looking from the M-bit section toward the L-bit section (C_L) becomes C_U, such that the functionality of the M-bit CDAC remains intact. The equivalent behavior of the split-CDAC is described in Fig. 2(c). While the M-bit CDAC has its original resolution, C_B works as an attenuator that exactly multiplies by $1/2^M$ so that the L-bit CDAC can resolve the output level after M-bits. Correspondingly, the total output voltage level considering all digital codes ($D_1 \sim D_{L+M}$) is obtained

$$\begin{aligned} V_{\text{out}} &= V_{\text{out},L} + V_{\text{out},M} \\ &= \left(\frac{\sum_{l=1}^{L} 2^{l-1} \cdot D_l}{2^{L+M}} + \frac{\sum_{m=1}^{M} 2^{m-1} \cdot D_{L+m}}{2^M} \right) \cdot V_{\text{ref}} \\ &= \frac{2^0 \cdot D_1 + 2^1 \cdot D_2 + \cdots + 2^{L+M-1} \cdot D_{L+M}}{2^{L+M}} \cdot V_{\text{ref}}. \end{aligned} \tag{2}$$

This result verifies that the two-section CDAC can effectively perform the $L + M$ bits of resolution.

Additional segmentation can be implemented in the last section of the segmented CDAC through the above process since it always terminates in a dummy capacitor; i.e., another section can be substituted for the dummy capacitor of the L-bit section. Fig. 3 shows a general MS-CDAC structure. Basically, the number of possible MS-CDAC cases depends on the target bits [# of possible cases $= 2^{(\#\text{ of bits})-1}$]. In this manner, MS-CDACs can be implemented in various section arrangements, denoted by "Cases," with different performance tradeoffs.

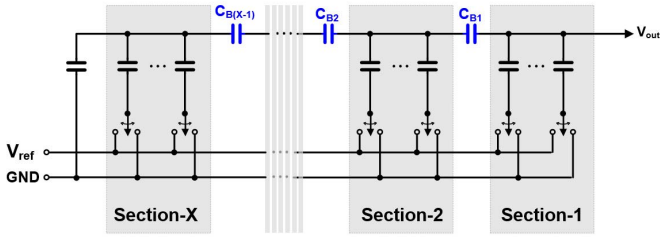


Fig. 3. General MS-CDAC structure.

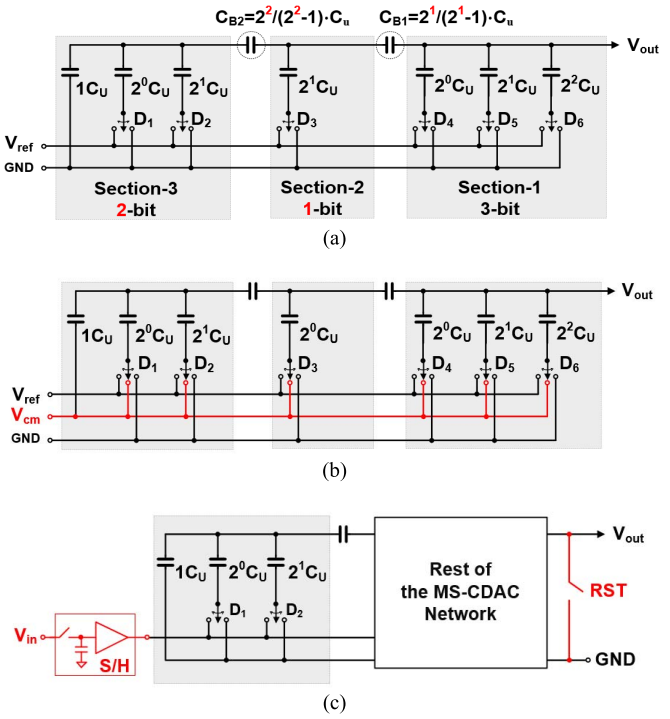


Fig. 4. Example of 6-bit MS-CDAC: Case-7 for (a) conventional switching, (b) V_{cm}-based switching, and (c) analog coefficient multiplier.

As a simplified investigation of the characteristics of MS-CDACs, this paper first studies a 6-bit MS-CDAC, hence having 32 possible cases. In Table I, every possible multi-section structure for 6-bit resolution is listed. Case-1 is the conventional single-section 6-bit CDAC. The section arrangements are presented in sequence such that the section including the MSB is the rightmost number (highlighted in red), and the section including the LSB is the leftmost number, which conforms to the section placement of the MS-CDAC circuits in this paper. The cases are grouped by the number of bits in the first section, which is equivalent to the rightmost numbers. For example, Case-7 is shown in Fig. 4(a), which has the section arrangement of {2–1–3}, thus belongs to group-3. Cases-2, 4, 8, 16, and 32 are equivalent to C–2C structures, and Case-5 is equivalent to the conventional two-section split-CDAC; thus, the MS-CDAC concept can be treated as inclusive of those other architectures. By having more options over the existing CDAC methods, the MS-CDAC allows for better optimized structures based on the fundamental tradeoff of static linearity and noise versus area, switching energy, and speed performance. It is straightforward to modify the MS-CDAC into V_{cm}-based switching scheme for low switching energy and linearity in SAR-ADC [11], [12], and to the coefficient multiplier, as shown in Fig. 4(b) and (c), respectively.

TABLE I
POSSIBLE CASES OF 6-BIT MS-CDAC

Case #	Group	Section Arrangement	Case #	Group	Section Arrangement
1	6	6	17	1	5-1
2	5	1-5	18		1-4-1
3	4	2-4	19		2-3-1
4		1-1-4	20		1-1-3-1
5	3	3-3	21		3-2-1
6		1-2-3	22		1-2-2-1
7		2-1-3	23		2-1-2-1
8		1-1-1-3	24		1-1-1-2-1
9	2	4-2	25		4-1-1
10		1-3-2	26		1-3-1-1
11		2-2-2	27		2-2-1-1
12		1-1-2-2	28		1-1-2-1-1
13		3-1-2	29		3-1-1-1
14		1-2-1-2	30		1-2-1-1-1
15		2-1-1-2	31		2-1-1-1-1
16		1-1-1-1-2	32		1-1-1-1-1-1

On the other hand, it becomes a challenging issue to find the optimized section segmentations among the large number of options in MS-CDACs with resolutions of 10 bit or above, typically seen in the SAR-ADC design. For example, a 10-bit MS-CDAC would have 1024 different section segmentations. As the combination of the sections is varied, it is prohibitively complicated to derive general design methods that cover every possible section arrangements. It is also infeasible to predict the performance just from the section segmentation. Therefore, detailed simulations and calculations for each section segmentation must be performed. In the case that the number of section segmentations is in the hundreds or even thousands, it would take an excessive amount of time to establish the optimized structure. Therefore, as a proof of concept, this paper first studies a 6-bit MS-CDAC structure in order to find its characteristics as a function of section segmentation. Subsequently, in Section IV, we proceed to the design of a higher resolution 10-bit MS-CDAC building on trends observed in the lower resolution structures.

III. CHARACTERISTICS AND TRADEOFFS OF 6-BIT MS-CDAC

In this section, the performance of all 32 cases of a 6-bit MS-CDAC is compared to find the characteristics as a function of the section segmentation. In a single-section CDAC design, overall performance is scaled with regards to the unit capacitor size. On the other hand, with the same unit capacitance, each case of the MS-CDAC may have different total capacitances, and it is necessary to understand how the overall performance varies. In this paper, Spectre simulations for MS-CDACs were employed to demonstrate the switching energy and static linearity performance of the MS-CDAC cases. Other parameters, such as input capacitance and total capacitance are obtained with straightforward calculations. This section provides a detailed performance comparison of the cases.

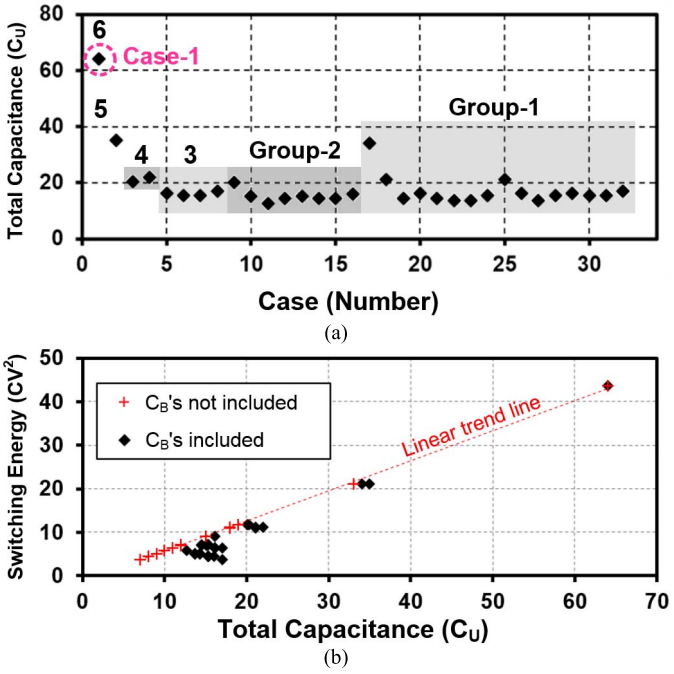


Fig. 5. (a) Total capacitance of MS-CDAC cases. (b) Switching energy versus total capacitance.

A. Total Capacitance and Switching Energy

Fig. 5(a) shows the total capacitance, which is the sum of all switched capacitors and also represents the overall area taken by capacitors not considering overhead area (space between capacitors), under the condition that all cases have the same unit capacitance. The range of the total capacitance is from $64C_U$ (Case-1) to $12.7C_U$(Case-11). It is observed that a larger number of sections, namely, more segmentation, do not guarantee lower area occupation. This is because when segmenting a 2-bit section into two 1-bit sections, more capacitor units are actually used since bridge capacitor is larger than the amount of unit capacitor saved by segmentation. The reduced total number of capacitor as well as the overall area helps reducing the cost, and routing complexity, which lessens the effect of parasitics from the layout.

Meanwhile, current is drawn into the CDAC from the supply at the digital code switching (D_1–D_6). This switching energy may represent a significant portion of the total power consumption in ultralow-power SAR-ADC applications [13] so needs to be considered to estimate the efficiency of MS-CDACs. In the conventional CDAC design, the switching power consumption is proportional to the unit capacitance. However, the section arrangement becomes an additional variable in MS-CDAC design. While the calculation of power consumption in single-section and split-CDACs are derived in [5] and [14] showing that split-CDAC helps reducing the switching power, it is quite complicated to calculate the energy consumed in every switching instance for MS-CDACs, so simulations are required. In the simulation environment, ideal capacitors and ideal switches were used at Cadence schematic level since switch resistance does not affect the switching energy and parasitic capacitances take only

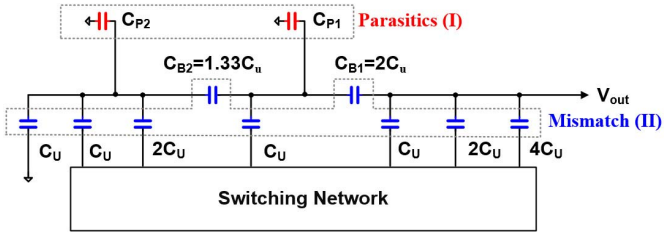


Fig. 6. Sources of nonlinearity (e.g., Case-7).

negligible portion of the energy [14]. Switching clocks are generated from ideal sources, and clock power consumption is not taken into account, as it is consistent regardless of the section arrangement.

After simulating energy consumption of all the binary switching output codes (64 numbers) in SAR-ADC operation, averaged values for each case were collected, and switching energy versus total capacitance, when C_B is considered or not considered in the total capacitance, is plotted in Fig. 5(b). Although bridge capacitors in each case need to be tuned for linearity, which will be introduced later in this section, the effect is negligible for both total capacitance and switching energy. It can be seen that switching energy is a highly proportional function of the total capacitance considering only switched capacitors. However, when C_Bs are counted in the total capacitance, some of the cases deviate from the linear relationship. This is mainly due to the fact that segmenting a 2-bit section requires less capacitance than two 1-bit sections. Correspondingly, segmenting a 2-bit section reduces switching energy but increases the total capacitance area. Leaving aside those minor exceptions, it is reasonable to conclude that both total capacitance area and switching energy generally benefit from the section segmentation. Compared to the single-section design (Case-1), up to 91% of energy consumption can be saved by a multisection structure with the same switching scheme.

B. Static Linearity

As previously stated, the main cost of the multisection structure is the degradation of static linearity. The sources of nonlinearities in an MS-CDAC are depicted in Fig. 6. The first nonlinearity factor (I) is due to top-to-ground parasitic capacitors, which are associated with the capacitors or wire lines. Parasitic capacitors do not degrade the nonlinearity in the single-section CDAC but only create gain error. The second nonlinearity factor (II) is the mismatch of the capacitors themselves. Capacitor variation is inversely proportional to the physical area of the capacitor; consequently, static linearity relies on the capacitor size in single-section CDAC design. In the MS-CDAC, the bridge capacitor is an additional critical contributor to nonlinearity, which leads to the inaccurate attenuation by the following sections. The bridge capacitor is typically a fractional unit value so it cannot be made by multiples of the unit capacitor, so must be individually sized as close as possible to the desired value, which increases the chance of mismatch with the other unit capacitors. Furthermore, the mismatch from bridge capacitors degrades static

linearity more significantly than the mismatch between the switched capacitors. Due to those additional factors of error, MS-CDAC has worse static linearity than the single-section CDAC as a tradeoff for reduced total capacitance.

Thanks to $V_{\rm cm}$-based switching, 6-bit MS-CDACs can be used in a 7-bit resolution SAR ADC. However, a 6-bit CDAC linearity analysis is still sufficient for both SAR-ADC and analog multiplier applications since static linearity of a 6-bit CDAC with conventional switching is identical to that of a 7-bit CDAC with $V_{\rm cm}$-based switching. For instance, let us assume that the voltage error is e_x in the 6-bit CDAC with a transition between [011111] and [100000], where "0" and "1" represent the GND and $V_{\rm ref}$, respectively, and LSB is the rightmost digit. Meanwhile, in $V_{\rm cm}$-based switching for 7-bit CDAC, there is [1/2 1/2 ... 1/2] between the former transition where "1/2 " represents $V_{\rm cm}(= 0.5V_{\rm ref})$. Both transition [011111] to [1/2 1/2 ... 1/2] and [1/2 1/2 ... 1/2] to [100000] have $e_x/2$ because all the voltage changes are halved. Since the LSB voltage level in the 7-bit DAC is half of that in the 6-bit DAC, the DNL of the 6-bit DAC with conventional switching and the 7-bit DAC with $V_{\rm cm}$ switching are the same. This characteristic agrees with the observation that $V_{\rm cm}$-based switching can achieve 2× lower DNL than the conventional switching for the same resolution [4].

Static linearity degradation from the top-to-ground parasitic capacitors ($C_{\rm P1}$ and $C_{\rm P2}$ in Fig. 6) can be compensated in nominal simulation (process variation neglected for the moment) by adjusting the bridge capacitor size. Parasitic capacitors in each section lead to more attenuation in the following sections rather than preceding sections resulting in positive DNL. To fix this nonlinearity, the bridge capacitors are increased to compensate for the attenuation. For example, let us assume that both top and bottom plates have 5% parasitic capacitance, and then C_{P1} and C_{P2} are $0.27C_U$ and $0.22C_U$, respectively. As a result, nominal simulation initially has a DNL, as shown in Fig. 7(a). Process variation is not considered so the resulting DNL is only caused by parasitic capacitors. It is seen that positive DNLs arise at the rising switching step of D_4([1110xx] to [0001xx]). By increasing the size of C_{B1} from $2C_U$ to $2.5C_U$ (25%↑), DNL can be improved as shown in Fig. 7(b), but the DNL value is pushed excessively in the negative direction. By adjusting C_{B1} down to $2.34C_U$, negative DNLs are compensated as shown in Fig. 7(c). Similarly, positive DNLs found at the rising switching step of D_3 ([110xxx] to [001xxx]) can be canceled out by increasing the size of C_{B2} from $1.33C_U$ to $1.42C_U$ (6.8%↑ from the original size). After this step, C_{B1} is a little bit reduced to $2.29C_U$(14.5%↑ from the original size) since the C_{B2} size creates small amount of negative DNL at the rising switching step of D_4. Consequently, overall DNL is minimized as shown in Fig. 7(d) with $|\text{DNL}|_{\max} < 0.01$ LSB. After eliminating the effect of the parasitic capacitance in this way, we can consider the remaining source of the nonlinearity, mainly the variability of the bridge capacitors

To estimate the static linearity taking capacitor mismatch into account, Monte Carlo (MC) simulations in Cadence were executed with the 6-bit MS-CDAC cases at the schematic level with vertical natural capacitors (VNCAPs) provided in

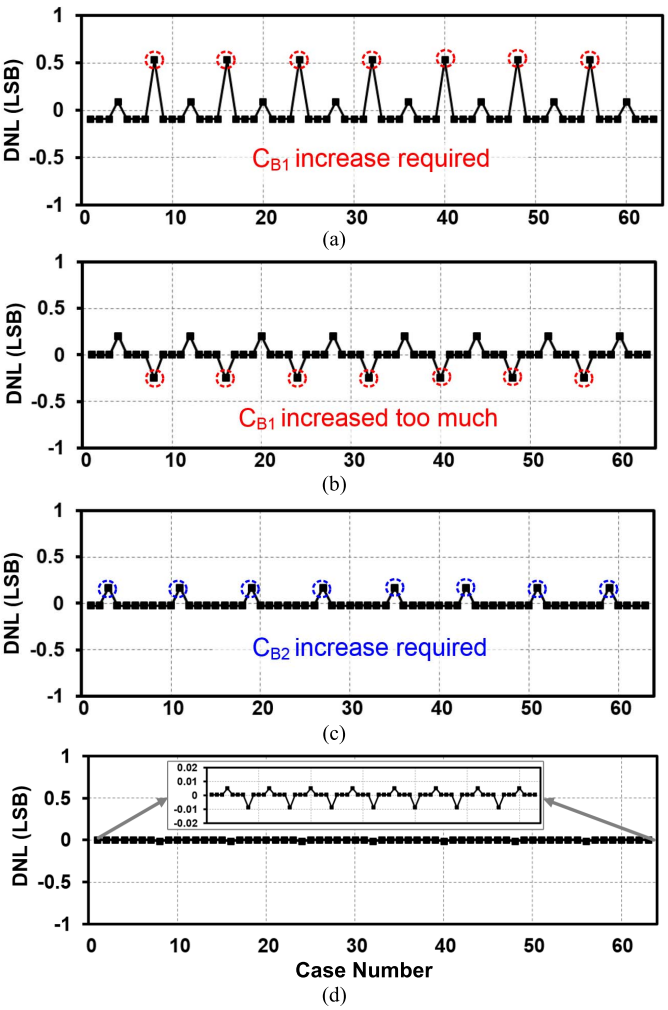


Fig. 7. Nonlinearity compensation steps. (a) Original DNL, (b) after increasing C_{B1}, (c) after readjusting C_{B1}, and (d) fixed DNL.

a 32-nm CMOS SOI process. Note that the VNCAPs in this technology have relatively poor capacitance variation ($\sigma \Delta C/C$), which is 1.5% in this technology, so they are not appropriate for high precision applications. Nonetheless, since the purpose of the 6-bit MS-CDAC case comparison is to find how section arrangement with the same unit capacitors affects the static linearity performance, it is helpful to use these VNCAPs to accentuate the differences in this paper. Parasitics of all 32 cases were compensated by adjusting bridge capacitors in nominal simulations as described above. As a result, |DNLs| are reduced to 0.05 LSB or less. Parasitic capacitance on the top and bottom plates of the capacitor is 8% and 5% each from the layout *RC* extraction. Interconnection routing may contribute to the parasitics but this can be also counteracted by the parasitic compensation. A total of 500 MC simulations were conducted for each case [15], and the 95% worst-case static linearity, i.e., the 25th largest $|\text{DNL}|_{\max}$ and $|\text{INL}|_{\max}$ values out of the 500 runs, were selected and plotted in Fig. 8. Case-1 (the single section case) has 0.30 and 0.18 LSB, respectively, and the other segmented cases all have worse values. INL is of relatively less concern than DNL in MS-CDAC cases. It is observed that the static linearity is highly correlated with the number of bits in the first section

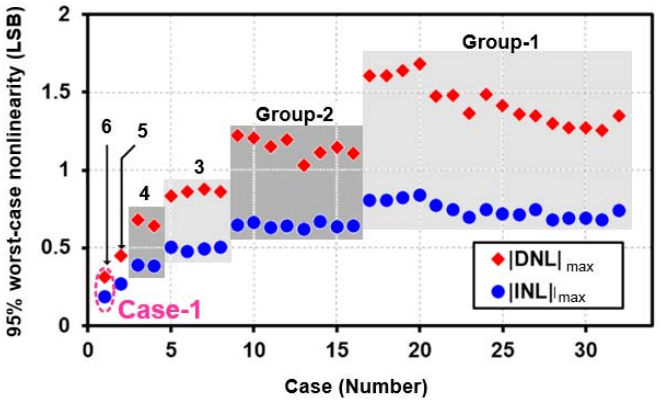


Fig. 8. Static linearity (DNL and INL) with respect to the 6-bit MS-CDAC cases.

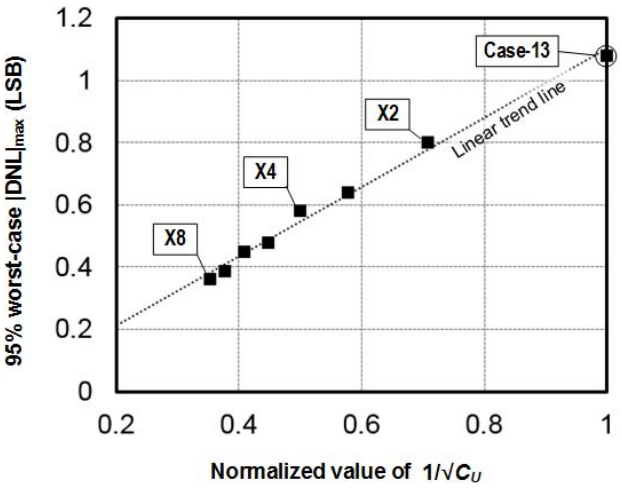


Fig. 9. Unit capacitor scaling versus 95% worst case $|\text{DNL}|_{\max}$ with 6-bit MS-CDAC (Case-13).

(group number); i.e., the cases with the larger number of bits in the first section have better static linearity. However, the arrangement of the following sections is less strongly correlated with the linearity performance.

It is also possible to scale the unit capacitor size in the MS-CDAC design to adjust nonlinearity. As the remaining factor of nonlinearity after parasitic compensation is almost entirely from capacitance variation, it is expected that nonlinearity of the MS-CDAC will be enhanced with the increase of unit capacitance size as with the single-section CDAC, which follows [16]:

$$\sigma_{\text{DNL,MAX}} \propto \frac{1}{\sqrt{A_{CU}}} \propto \frac{1}{\sqrt{C_U}} \tag{3}$$

where $\sigma_{\text{DNL,MAX}}$ denotes the standard deviation of the maximum DNL of the single-section DAC and A_{CU} is the area of unit capacitor, correspondingly unit. To verify that (3) is valid for MS-CDACs as well, another set of MC simulations is run for Case-13, {3–1–2}, with unit capacitor scaling from 1 to 8 times and the result is shown in Fig. 9. The simulation results prove that $|\text{DNL}|_{\max}$ is predictable as a linear function of $1/\sqrt{C_U}$. It should be noted that scaled MS-CDACs have increased total capacitance, switching energy, and MSB section capacitance with the same scaling ratio, thus need to be compared with nonscaled structures considering those changes.

C. Sampling Noise and Speed

Both sampling noise and speed are determined by the number of bits in the first section, which is referred to as the group number of the MS-CDAC (see Table I). In SAR-ADC applications with V_{cm}-based switching scheme, the input signal is sampled on the top plates of the first section. Thus, the input capacitance, which is the sum of capacitors in the first section, i.e., twice the MSB capacitor, must be sufficient to meet kT/C noise requirements resulting in

$$\frac{kT}{C_S} < \left(\frac{V_{\text{ref}}}{\sqrt{12}\cdot 2^N}\right)^2 \tag{4}$$

where N is the number of bits, and C_S is the sampling capacitance [3].

On the other hand, the MSB capacitance, which is also determined by the group number, must be minimized for higher speed. This is because SAR-ADCs suffer the worst-case settling time at the MSB switching, and analog coefficient multipliers see a maximum capacitance load of half-MSB capacitance. For instance, group-4 cases have about 2× longer settling time than group-3 cases due to 2× larger MSB capacitor. The section segmentation in MS-CDACs effectively reduces the MSB capacitance, and the following sections do not affect the speed as capacitance looking from output to the following sections is always seen as a unit capacitance. In addition, parasitics including the interconnection resistance and capacitance can also be factors in reducing the speed. The reduced number of capacitor units in MS-CDAC mitigates the effect of parasitics. It can be also observed that the settling time is also roughly in tradeoff relationship with the static linearity (Fig. 8).

D. Overall Tradeoffs in 6-Bit MS-CDAC Cases

The studied MS-CDAC cases present various characteristics of total capacitance, switching energy, and static linearity. In order to observe the fundamental tradeoff, total capacitance versus static linearity is plotted in Fig. 10. Note that the total capacitance is not only related to the area but also determines switching energy; both area and switching speed are improved by section segmentation, whereas the static linearity is degraded. In addition, we can also examine speed and noise performance based on the group number. A reference line is drawn on the plot that connects the cases (1–6 and 11) that are considered "optimal" in terms of the number of capacitor units versus linearity tradeoff. The cases other than optimal are considered comparatively inefficient; i.e., they have inferior linearity for the total capacitance. For example, Case-17 has poor linearity although total capacitance is only slightly less than Case-2. The reference line approximately shows that DNL is inversely proportional to total capacitance. This result is similar to the scaling of a single-section CDAC, which follows (3).

TABLE II
PERFORMANCE OF OPTIMAL 6-BIT CASES

Case	*1*	*2*	*4*	*3*	*5*	*6*	*11*	*31*	*27*
Section	6	1-5	1-1-4	2-4	3-3	1-2-3	2-2-2	2-1-1-1-1	2-2-1-1
Group	6	5	4	4	3	3	2	1	1
Total Capacitance (C_U)	64 (-)	35 (-45%)	22.0 (-66%)	20.3 (-68%)	16.1 (-75%)	15.3 (-76%)	12.7 (-80%)	15.3 (-76%)	13.7 (-79%)
Switching E (CV_2)	43.6 (-)	21.1 (-52%)	11.7 (-73%)	11.1 (-74%)	9.0 (-79%)	7.1 (-84%)	5.7 (-87%)	4.4 (-90%)	5.1 (-88%)
95% worst-case $\|DNL\|_{max}$ (LSB)	0.31 (-)	0.45 (+0.13)	0.60 (+0.33)	0.63 (+0.37)	0.84 (+0.52)	0.86 (+0.55)	1.15 (+0.84)	1.25 (+0.84)	1.35 (+0.55)
95% worst-case $\|INL\|_{max}$ (LSB)	0.19 (-)	0.27 (+0.08)	0.38 (+0.20)	0.39 (+0.21)	0.50 (+0.32)	0.48 (+0.29)	0.63 (+0.45)	0.68 (+0.50)	0.74 (+0.56)
Input C (C_U)	64, 16 (-)	32, 8 (-50%)	16, 4 (-75%)	16, 4 (-75%)	8, 2 (-88%)	8, 2 (-88%)	4, 1 (-94%)	2, 0.5 (-97%)	2, 0.5 (-97%)
*Scaling factor**	N/A	N/A	1.6	1.8	2.8	3.0	5.3	6.3	7.3
Total Capacitance after scaling	N/A	N/A	36	38	45	45	67	96	100

* Unit capacitor scaling to achieve 0.5 LSB of 95% worst-case $|DNL|_{max}$.

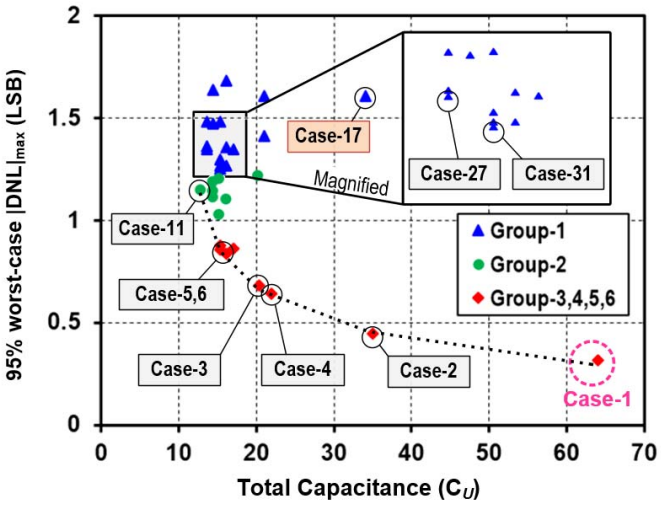


Fig. 10. Total capacitance versus DNL. Optimal cases are selected based on total capacitance and MSB capacitance (group) versus DNL.

As mentioned before, speed and noise performances can be estimated by the group numbers. In Fig. 10, the optimal cases have lower group numbers as the total capacitance decreases, which means better speed but degraded noise performance, consistent with reducing the unit capacitance in single-section CDAC.

Based on the above observations, it can be seen that the MS-CDAC offers similar performance tradeoffs as the single-section CDAC with unit capacitor sizing. In other words, MS-CDAC can be used to extend the fundamental tradeoff when the minimum capacitor size is the bottleneck of the design. Table II provides the detailed performance of the optimal cases including the change relative to Case-1, which represents the design limit of a single-section CDAC based on the available minimum size unit capacitor. Although none of the group-1 cases are on the reference line, it is still worthwhile to consider them for better settling time. Among the cases of group-1, Cases-27 and 31 can be considered optimal as well and are shown in Table II.

As discussed before, with the given options of section segmentation, it is possible to consider unit capacitor scaling of the MS-CDAC to further optimize the structure. While Cases-1 and 2 cannot have further reduced total capacitance, unit capacitance of the other cases can be increased to fulfil the requirement. Based on (3), required unit capacitor scaling to enhance current $|DNL|_{max}$ to 0.5 LSB can be calculated for each MS-CDAC structure as follows:

$$C_{U,\text{scaled}} = \left(\sqrt{C_{U,\min}} \cdot \frac{|\text{DNL}|_{\max}}{0.5}\right)^2. \tag{5}$$

In Table II, calculated total capacitance, after unit capacitor scaling based on (5), for each case is included. We can observe that as an MS-CDAC structure with minimum unit capacitor deviates further from desired nonlinearity, it requires larger factor of unit capacitor scaling, resulting in larger total capacitance. After scaling for the same condition of static linearity, the total capacitance of Case-4 is the least ($36C_U$), Case-5 ($45C_U$) is the next, and Case-11 is the largest ($67C_U$). This order matches with the scaling factor. This relationship holds true between the other scaling-required section segmentations as well, since reducing total capacitance by the section segmentation is more strongly traded against linearity than unit capacitance scaling due to the bridge capacitor variation. Therefore, among the scaling-required MS-CDACs, it is desirable to choose the case that needs the least scaling factor. After consideration of unit capacitor scaling, the optimal scaled case needs to be compared with the optimal nonscaled case since it may have smaller total capacitance.

If we consider selection of 6-bit MS-CDAC based on the collected results shown in Table II, Case-2 and Case-4 can be chosen, as they represent optimal choices among scaled and nonscaled cases, respectively. After finding a comparable section segmentation, selection could be dependent on designer's choice. Case-2 with the minimum unit capacitor can be selected for slightly better total capacitance for area and switching energy. On the other hand, Case-4 is chosen for a bit better speed performance since Case-4 has X0.8 ($= 0.5 \times 1.6$) of the MSB section capacitance after scaling. If the number of

TABLE III
CONSIDERATIONS OF MS-CDAC PERFORMANCE IN SAR-ADC AND ANALOG COEFFICIENT MULTIPLIER

	SAR-ADC	Analog Coefficient Multiplier
Capacitance Mismatch	Static linearity	Coefficient selection
kT/C noise	Considered	Not considered
Switching Energy	Considered	Not considered
Area	Considered	Considered
Speed	Considered	Considered

unit capacitors is a concern, Case-4 is preferred as it provides about 40% less number of units regardless of the scaling than Case-2.

E. Considerations in SAR-ADC and Analog Coefficient Multiplier Applications

The tradeoff considerations are applied differently depending on whether the CDAC is being used in an SAR-ADC or as a coefficient multiplier for analog signal processing. Table III shows the consideration of various performance criteria in each application. Essentially, SAR-ADC design requires consideration of all criteria. On the other hand, analog coefficient multipliers [17] do not consider kT/C noise because the input signal is sampled on the previous stage, which is a sample and hold. Instead, the speed of the multiplier is associated with the maximum input capacitance. Thus, the number of bits in the first section is not limited by noise, but rather by static linearity.

The static linearity in the coefficient multiplier does not create any quantization noise or unwanted harmonics as would be of concern in an ADC. Instead, the coefficient control resolution may limit the arithmetic accuracy of the analog signal processing, such as the accuracy of the transfer function of an analog finite-impulse response filter. Switching energy is not also critical in analog coefficient multipliers because the current drawn into the capacitor is negligible compared to the static current of the S/H buffer as well as the other blocks in the overall circuit.

IV. TEN-BIT MS-CDAC DESIGN

To verify the concept of MS-CDAC in a more practical application, the use of MS-CDAC structures is extended to a medium resolution, typical of SAR-ADC applications. This section presents the design of a 10-bit MS-CDAC as a proof of concept. As mentioned earlier, a major issue with higher resolution designs is a very large number of possible cases; there are 1024 possible section arrangements for a 10-bit MS-CDAC. This large number of options provides a greater trade space to optimize the CDAC design but it is prohibitively time-consuming to compare all the possible section arrangements as was done for the simpler 6-bit

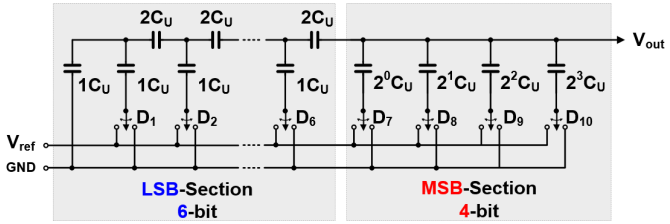


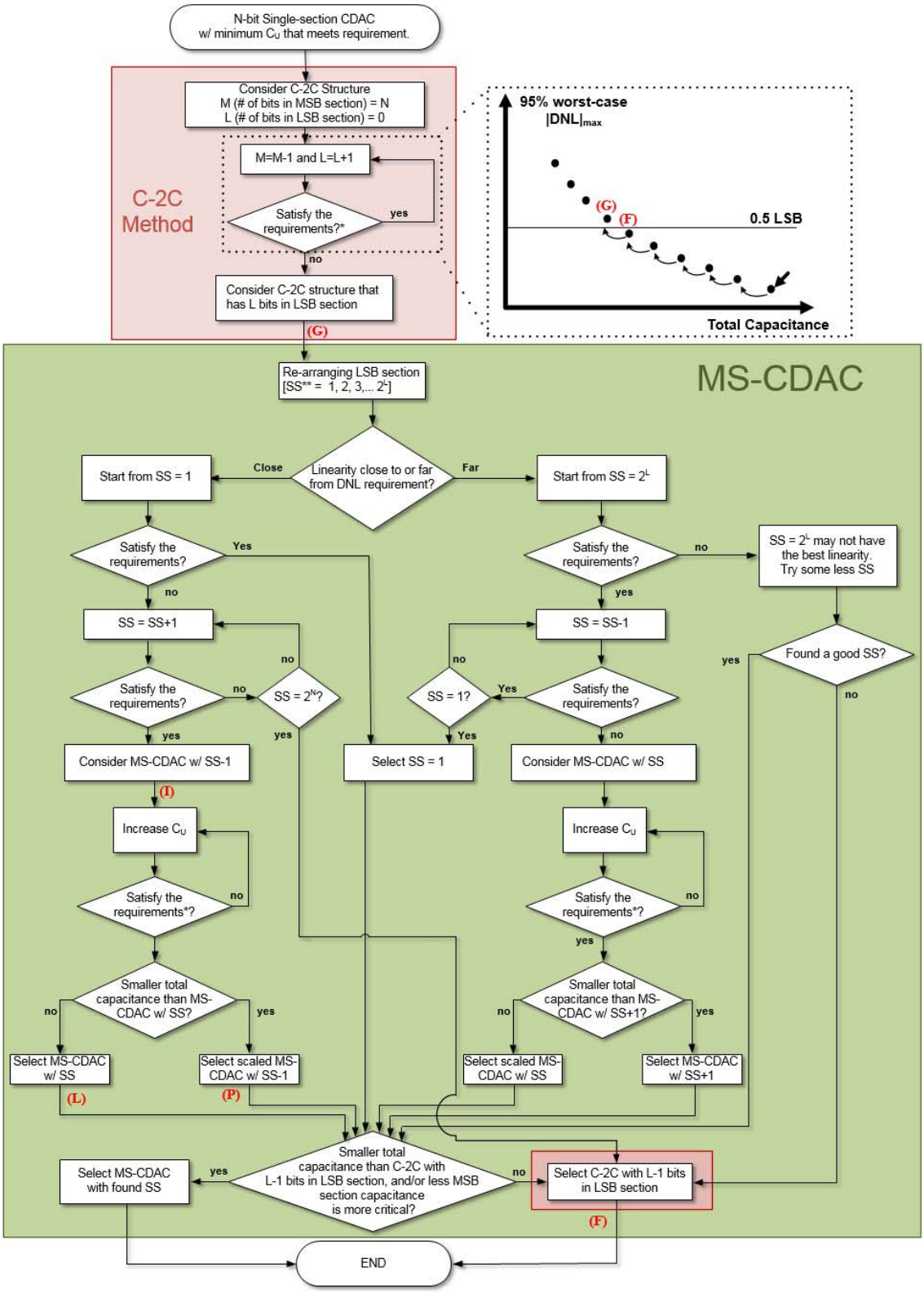
Fig. 11. 10-bit C–2C structure with 4-bit MSB section and 6-bit LSB section.

example discussed above. Along with the number of section arrangements, the time required to analyze or simulate each section arrangement increases exponentially due to the growth of the capacitor unit count and complexity.

In order to provide a more efficient design process, this paper presents a 10-bit MS-CDAC design without analyzing all possible structures by considering a C–2C architecture (Fig. 11) as an intermediate stage of the design. This design flow is shown in Fig. 12. The single-section CDAC can be turned into C–2C architecture by incrementally adding C–2C bits. As more bits are implemented by C–2C pairs in the LSB section, the total capacitance is reduced while the static linearity and noise are degraded (see total capacitance versus 95% worst-case $|\text{DNL}|_{\max}$ graph inset in Fig. 12). By incrementally adding more bits to the C–2C structure until the section arrangement just fails to meet the requirement [(G) in Fig. 12], we can find the optimal C–2C structure [(F) in Fig. 12] that satisfies the requirement with minimum total capacitance ($L-1$ bits in the LSB section). Next, the C–2C structure with L-bit LSB section is considered for MS-CDAC implementations by modifying the LSB section. In other words, in the MS-CDAC design, the C–2C method helps to first converge on an appropriate number of bits in the first section, since this plays a critical role in the static linearity and noise performance. Consequently, the possible section arrangements are reduced to 2^L from 2^N.

In MS-CDAC section arrangement search process (presented in the shaded green box in Fig. 12), possible section arrangements are represented as "SS" numbering in the order of the total capacitance size from 1 to 2^L. We need to first determine whether to start searching from the largest (SS $=$ 1) or the smallest (SS $= 2^L$) total capacitance case in order to minimize the design time. If the C–2C structure with an L-bit LSB section has DNL performance close to the requirement, the former is appropriate; if the DNL performance is further from the requirement; then, the latter is appropriate. Like the preceding C–2C structure search, an optimized section arrangement can be determined by simulating the possible section arrangements in either increasing or decreasing the total capacitance order. As discussed before, scaling may lead to better performance. Thus, the section arrangement that has the next smaller total capacitance is scaled and compared to the optimal nonscaled section arrangement.

The optimal MS-CDAC structure resulting from this search process still needs to be compared with the optimal C–2C structure since it may have larger total capacitance. If the optimal MS-CDAC structure has the smaller total capacitance or even if the MS-CDAC structure has larger total



* Requirements of kT/C noise and DNL

** Numbering possible section segmentation from smallest to largest.

Fig. 12. Design flow of the MS-CDAC design from intermediate C–2C cases. (·) refer to the 10-bit design cases shown in Table IV.

capacitance but the MSB section capacitance is more critical, the optimal MS-CDAC structure becomes the final selection. In the case that there is no MS-CDAC case considered that satisfies the requirement, we can also choose the optimal C–2C structure. The detailed design of a 10-bit MS-CDAC using the proposed method follows.

TABLE IV
95% WORST-CASE $|DNL|_{max}$ OF 10-BIT C–2C AND MS-CDAC STRUCTURES

Architecture Method	Case	Section Arrangement	Total Cap. (C_U)	95% worst-case $|DNL|_{max}$ (LSB)	Total Cap. After scaling (C_U)
C-2C	A	10	1024	0.04	N/A
	B	1-9	515	0.06	N/A
	C	1-1-8	262	0.10	N/A
	D	1-1-1-7	137	0.16	N/A
	E	1-1-1-1-6	76	0.21	N/A
	F	1-1-1-1-1-5	47	0.40	N/A
	G	1-1-1-1-1-1-4	34	0.73	72
	H	1-1-1-1-1-1-1-3	29	1.37	218
MS-CDAC	I	2-2-2-4	30	0.76	69*
	J	2-2-1-1-4	31.7	0.43	N/A
	K	2-1-2-1-4	31.7	0.42	N/A
	L	1-2-2-1-4	31.7	0.40	N/A
	M	1-1-2-2-4	31.7	0.78	77
	N	1-2-1-2-4	31.7	0.68	59
	O	2-1-1-2-4	31.7	0.61	47

* Case-P, which is scaled Case-I for the static linearity.

For the 10-bit MS-CDAC design, a 130-nm CMOS technology is utilized, with MIM capacitors available having 17 fF of minimum capacitance. This unit capacitor has 0.06% capacitance variation ($\sigma \Delta C/C$). Table IV shows the results of 500 MC simulation runs in Cadence with MS-CDACs implemented at the schematic level for the purpose of searching the optimal section segmentation. Single-section CDAC achieved less than 0.05 LSB of 95% worst-case $|DNL|_{max}$ (Case-A) and 17.4-pF input capacitance with the minimum-sized unit capacitor, which greatly exceeds the requirement. Accordingly, we can pursue the MS-CDAC structure per the proposed design flow.

Next, the single-section CDAC is transformed by segmenting the capacitor array from the LSB section. In Table IV, 95% worst-case $|DNL|_{max}$ values from 500 MC simulations runs for 10-bit C–2C arrangements are shown. Up to 7 bits of C–2C structures are simulated. It is seen that Case-F (5-bit MSB) would be chosen to have less than 0.5 LSB of $|DNL|_{max}$ if only the C–2C method is considered (see Case-F in Fig. 12). However, for MS-CDAC, Case-G (5-bit MSB C–2C arrangement) can be also considered since it has $|DNL|_{max}$ not very far from the desired value, and it is possible to have improved static linearity by modifying the LSB section into different section arrangements (see Case-G in Fig. 12). The input capacitance (272 fF) is also above the requirement. Meanwhile, the 7-bit LSB version of the C–2C structure has a more degraded DNL, and its input capacitance (136 fF) is not sufficient to meet kT/C noise requirements. Due to the fewer bits of the first section, the 4-bit MSB C–2C inherently has about $\sim 2\times$ faster speed and can achieve much less area/switching energy than the possible 5-bit MSB section cases. Therefore, we seek to find an MS-CDAC case to replace the 6-bit LSB section of the C–2C.

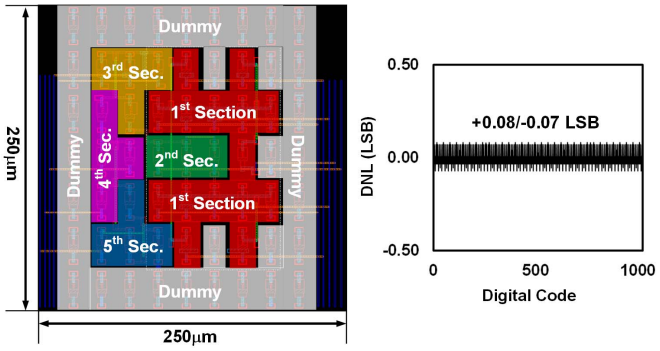


Fig. 13. Layout of Case-L and the result of postlayout static linearity simulation.

As the number of bits in the first section is fixed, the number of possible options is largely reduced (by a factor of X16). Furthermore, it is not necessary to attempt all possible section arrangements with remaining 6 bits. In Section III, it is found that $|DNL|_{max}$ tends to increase as total capacitance decreased. With that result in mind, we can examine the possible section arrangements of the total capacitance from either smallest case to largest case or vice versa, until the desired structure is found. Since $|DNL|_{max}$ of a 6-bit LSB section C–2C is not too far from the desired value, it is preferred to search from the smallest total capacitance case. Table IV also provides the simulated $|DNL|_{max}$ values from the smallest total capacitance of section arrangement {2–2–2–4}, which is Case-I. The optimal nonscaled section arrangement turns out to be Case-L (see Case-L in Fig. 12). Cases-J and K also satisfy the condition and very close to Case-L. While it is possible that simulation inaccuracies may lead to the slight difference, it is not critical issue since they all achieve $|DNL|_{max}$ value fairly less than the required value and have the same total capacitance.

The section segmentation of the next smaller total capacitance is Case-I, so it is scaled to see if it has smaller total capacitance after scaling. As shown in Table IV, if Case-I is scaled, i.e., Case-P (see Case-P in Fig. 12), it has larger total capacitance than nonscaled Case-L. Due to the scaling with over a factor of 2, the MSB section capacitance is also inferior to Case-L. Overall, the optimal MS-CDAC section arrangement is Case-L for less than 0.5 LSB of $|DNL|_{max}$.

Since interconnect routing in physical layout introduces additional parasitics, it is necessary to understand the impact of layout parasitics on the MS-CDAC performance. In order to fully verify the feasibility of the proposed approach, the postlayout simulations were conducted. Fig. 13 shows the layout design of the Case-L design in a 250 μm $\times$ 250 μm die area using the available 130-nm CMOS technology. As additional top-to-ground parasitic capacitance causes more attenuation in each section, the bridge capacitor values must be increased correspondingly. After the bridge capacitor adjustments, the postlayout simulation results in $<$0.1 LSB of $|DNL|_{max}$, which is only $<$0.05 LSB worse than the prelayout simulation.

TABLE V
PERFORMANCE COMPARISON OF SELECTED 10-BIT MS-CDAC WITH OTHER EXISTING METHODS

Architecture	Case	Section Arrangement	Total Cap (C_U)	Switching E (CV^2)	# of capacitors	95% worst-case $\|INL\|_{max}$ (LSB)	95% worst-case $\|DNL\|_{max}$ (LSB)	First section Bit #
Single Section CDAC	A	10	1024	761.4	1024	0.04	0.04	10
Split-CDAC	-	5-5	64.0 (-94%)	46.8 (-94%)	64	0.16 (-0.13)	0.25 (-0.21)	5
C-2C (5LSB-5MSB)	F	1-1-1-1-1-5	47 (-95%)	27.4 (-96%)	47	0.29 (-0.25)	0.40 (-0.35)	5
Selected 10-bit MS-CDAC	L	**1-2-2-1-4**	**30.7 (-97%)**	**17.4 (-98%)**	**30**	**0.29 (-0.25)**	**0.40 (-0.35)**	**4**

Table V shows the comparison of the selected MS-CDAC structure with split, C–2C and single-section CDAC cases. All of those are designed with the same unit capacitors but only section arrangements are different. It is observed that the selected 10-bit MS-CDAC architecture achieves 97% lower total capacitance, 98% lower switching energy, about a factor of 30 fewer capacitor units, and only 4 first-section bits, while still achieving acceptable static linearity. In addition, having a factor of ∼30 fewer capacitor units greatly simplifies the routing in layout. At the same time, it is also shown that the MS-CDAC outperforms the conventional methods under the given requirements for a 10-bit CDAC. The selected MS-CDAC has 35% lower total capacitance, as well as 36% lower switching energy compared to the split-CDAC and C–2C designs. Above all, the first section is reduced to 4 bit, which could not be attained by the other methods. This result proves that MS-CDAC design leveraging the intermediate C–2C method effectively leads to optimized section arrangement selection, avoiding excessive number of options. Although a specific number of bits and capacitor type using a specific technology are used in this analysis, the method to find the optimal section segmentation can be generally applied to other technologies and applications.

V. CONCLUSION

The MS-CDAC has been investigated as a technique to optimize CDAC structures for analog multiplier and SAR-ADC applications. It is first observed that a CDAC can be transformed into multiple sections by replacing a dummy transistor with additional capacitor array(s) using bridge capacitor(s). In order to understand the characteristics of MS-CDAC depending on the section segmentation, calculations, and simulation of all possible section arrangements for a low resolution (6 bit) MS-CDAC were conducted. These different section segmentations have similar tradeoffs of total capacitance, switching energy, speed versus static linearity, and noise as the sizing of unit capacitance in single-section (conventional) CDAC. Therefore, we can use MS-CDAC in order to optimize the performance by finding the section segmentation with minimum total capacitance while the required conditions of linearity and kT/C noise are met.

To present a practical application of MS-CDAC concept, a 10-bit MS-CDAC design is presented. It is shown that a desirable section arrangement can be found by searching candidate C–2C structures first, and then modifying the LSB section using the MS-CDAC approach, instead of considering all 1024 options of the 10-bit structure. Following this procedure, targeting <0.5 LSB of $|DNL|_{max}$ for 95% of 500 MC simulation runs, the selected 10-bit MS-CDAC accomplishes 97% reduction of total capacitance and 98% reduction of switching energy as well as minimized input capacitance for speed. This achievement is more than 30% better than C–2C and split-CDAC methods. In addition, the number of bits in the first section is 1 bit reduced which can result in about 2× lower settling time. The postlayout simulation further validates the approach; the selected MS-CDAC performance is <0.1 LSB of $|DNL|_{max}$ after the effect of additional parasitics from the layout is compensated by adjusting the bridge capacitors. In the future work, this MS-CDAC technique will be applied to wideband reconfigurable analog signal processing circuits currently under development.

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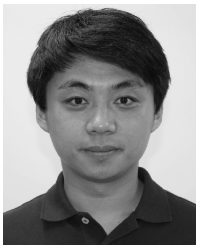

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